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# Anisotropic plasma etching of Silicon in gas chopping process by alternating steps of oxidation and etching

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## Abstract

Gas chopping plasma etching of Silicon is well known process providing deep anisotropic etching of microstructures for MEMS applications, TSV for 3D integrations of ICs etc. It includes the alternative steps: the passivation of surface sidewalls and then etching the bottom of structure. Polymerizing fluorocarbon based plasmas of 4F8 (CHF<sub>3</sub>) gas is used at passivation step in Bosch process C4F8 / SF<sub>6</sub> giving C<sub>x</sub>F<sub>y</sub> polymer film on surface. After completing of microstructure etching the polymer layer should be removed from sidewalls by additional plasma stripping and wet chemistry operations.

There exists more clean cryogenic deep silicon etching processes. First version is continuous regime with SF<sub>6</sub>+O<sub>2</sub> plasma and the second is gas chopping process SF<sub>4</sub>+O<sub>2</sub>/SF<sub>6</sub> which is patented as STiGer etch process. Both processes requires cooling the Silicon wafer up to -100°C and utilizes the SixFyOz passivation layer stable at cryogenic temperature. This layer completely evaporates at room temperature after etching.

Obviously, the temperature stability of SixFyOz film depends on content of fluorine, and without fluorination the SiO<sub>x</sub> film is remarkably stable at rt and higher temperatures. In the present work a two-stage process for deep etching of Silicon based on alternating steps of etching in SF<sub>6</sub> plasma and Silicon oxidation in O<sub>2</sub> plasma is proposed. This developed Ox-Etch process has advantages of free from deposited polymers and does not use cryogenic equipment.

Processes were performed at room temperature in plasma etchers with high density ICP plasma source (RF frequency of 13.56 MHz and 2 MHz was used, RF power 800 – 1750 Watt) at chamber pressures of 5-30 mTorr. Wafer bias was in range of 30 – 50 V during etching step, and 0-30 V during oxidation step. Experiments were carried out on Silicon wafers(100) (n-type, 10-20 Ohm•cm). Hard mask of SiO<sub>2</sub> layer of 1-2 μm was made by lithography with test topology of cylindrical holes and lines sized at 2-75 μm.

Silicon oxidation by O<sub>2</sub> plasma was studied by *in situ* spectral ellipsometry on bare wafer surface during Oxy-step of process. It was shown that without D bias the oxide film grows up to 5 nm within time of 3-5 seconds. Under bias of 30-60 V oxide thickness saturates at 5-7 nm where growth of SiO<sub>x</sub> stops due to balance between oxidation and ion sputtering rates. The main condition for success of Ox-Etch gas chopping process implies that reduction in sidewall oxide thickness during the etching step should be compensated during following oxidation step. Typical duration of passivation and etching steps do not exceed 10 sec, and the mean etch rates of Silicon up to 3 μm/min are achievable without noticeable undercut.

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Etched structures show anisotropic profile with vertical scalloped walls similar to Bosch and STiGer processes. Selectivity of Silicon etching with respect to silicon oxide mask is up to 20:1. Main controlling parameters for Ox-Etch process which determines the etch rate and degree of anisotropy are the duration of stages. The investigations on etching rates, aspect-dependent etching, and sidewall roughness are presented.

Ox-Etch process could be applied to application where contamination of Silicon walls after etching could be a critical obstacle. After Ox-Etch process the passivation layer on walls of microstructures is close to native SiO<sub>2</sub>.

To reduce the bombardment of the sidewalls by scattered ions it is essential to use low pressure discharge (2-10 mTorr) and a sufficient plasma density. Therefore, the process could be realized only in reactors with HDP-sources of plasma.